Amendments to the Claims

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A DSP (Digital Signal Processing) architecture with a wide memory bandwidth, the DSP architecture comprising:

a first communication port;

first, second, and third memory devices, which are connected with the first communication port and are arranged in a first row direction of the DSP architecture;

a fourth memory device, a calculation element, and a fifth memory device, which are arranged in a second row direction below the first row direction of the DSP architecture; and

sixth, seventh, and eighth memory devices, which are connected with the first communication port and arranged in a third row direction of the DSP architecture,

wherein the calculation element is surrounded by the first through the ~~eight~~ eighth memory devices and is directly connected with each of the first through the ~~eight~~ eighth memory devices.

2. (Original) The DSP architecture of claim 1, further comprising a second communication port, which is connected with the first, the fourth, and the sixth memory devices arranged in a first column direction of the DSP architecture, and with the third, the fifth, and the eighth memory devices arranged in a third column direction of the DSP architecture.

3. (Previously Presented) The DSP architecture of claim 2, wherein the second and seventh memory devices are connected to the second communication port through the calculation element and arranged in a second column direction of the DSP architecture.

4. (Original) The DSP architecture of claim 3, wherein the second column direction is disposed between the first and the third column directions.

5. (Original) The DSP architecture of claim 4, wherein the second row direction is

disposed between the first and the third row directions.

6. (Original) The DSP architecture of claim 1, wherein the calculation element and the first through the eighth memory devices form one arrangement unit, wherein the calculation element is disposed in the center of the arrangement unit, the first through the eighth memory devices are connected to the calculation element, and the arrangement unit is arranged in row directions and column directions of the DSP architecture.

7. (Withdrawn) A memory mapping method to process an image, which is used in a DSP architecture, the method comprising:

storing data received through a first communication port in first and second memory devices arranged in a first row direction of the DSP architecture;

storing the data received through the first communication port in a third memory device arranged in a second row direction of the DSP architecture, wherein the data is stored in the third memory device, through a first calculation element that is connected with the first and the second memory devices and neighboring with the third memory device in the second row direction; and

processing the data stored in the first through the third memory devices using the first calculation element.

8. (Withdrawn) The memory mapping method of claim 7, comprising:

storing the data processed by the first calculation element in a fourth memory device neighboring with the second memory device in the first row direction of the DSP architecture, and in a fifth memory device neighboring with the first calculation element in the second row direction of the DSP architecture; and

processing the data stored in the fourth and the fifth memory devices using a second calculation element neighboring with the fifth memory device in the second row direction of the DSP architecture.

9. (Withdrawn) A memory mapping method to process an image, which is used in a DSP architecture, the memory comprising:

storing data received through a first communication port in first and second memory devices arranged in a first row direction of the DSP architecture;

storing the data received through the first communication port in fourth and fifth memory devices arranged in a third row direction of the DSP architecture;

storing the data received through the first communication port in a third memory device arranged in a second row direction of the DSP architecture, wherein the data is stored in the third memory device, through a first calculation element connected with the first and the second memory devices and neighboring with a third memory device in the second row direction;

storing the data received through the first communication port in a sixth memory device arranged in a fourth row direction of the DSP architecture, wherein the data is stored in the sixth memory device, through a second calculation element connected with the fourth and the fifth memory devices and neighboring with the sixth memory device;

processing the data stored in the first through the third memory devices using the first calculation element; and

processing the data stored in the fourth through the sixth memory devices using the second calculation element.

10. (Withdrawn) The memory mapping method of claim 9, further comprising:

storing the data calculated by the first calculation element in a seventh memory device neighboring with the second memory deice in the first row direction of the DSP architecture, and in an eighth memory device neighboring with the first calculation element in the second row direction of the DSP architecture;

processing the data stored in the seventh and the eighth memory devices using a third calculation element neighboring with the eighth memory device in the second row direction of the DSP architecture;

storing the data calculated by the second calculation element in a ninth memory device neighbouring with the fifth memory device in the third row direction of the DSP architecture, and in a tenth memory device neighboring with the second calculation element in the fourth row direction of the DSP architecture; and

processing the data stored in the ninth and the tenth memory devices using a fourth calculation element neighboring with the tenth memory device in the fourth row direction of the

DSP architecture.

11. (Original) A memory mapping method to process an image, which is used in a DSP architecture, the method comprising:

storing data received through a first communication port in first, second, and third memory devices arranged in a first row direction of the DSP architecture, or in sixth, seventh, and eighth memory devices arranged in a third row direction of the DSP architecture;

storing data received through a second communication port in the first and the sixth memory devices and a fourth memory device that are arranged in a first column direction of the DSP architecture, or in the third and the eighth memory devices and a fifth memory device that are arranged in a third column direction of the DSP architecture; and

processing the data stored in the first through the eighth memory devices, using a calculation element disposed between the fourth and the fifth memory devices arranged in a second row direction of the DSP architecture and between the second and the seventh memory devices arranged in a second column direction of the DSP architecture.

12. (Currently Amended) A DSP (Digital Signal Processing) architecture with a wide memory bandwidth, the DSP architecture comprising:

a first communication port to receive data;

at least three memory devices connected with the first communication port and arranged in a first row direction of the DSP architecture to temporarily store at least a first portion of the data received at the first communication port;

at least two memory devices arranged in a second row direction below the first row direction of the DSP architecture;

at least three memory devices connected with the first communication port and arranged in a third row direction of the DSP architecture to temporarily store at least a second portion of the data received at the first communication port; and

a calculation element connected with each of the memory devices of the first, second and third rows of the DSP architecture to process and transfer the first portion of the data temporarily stored in the at least three memory devices in the first row and to process and transfer the second ~~portions~~ portion of the data temporarily stored in the at least three memory

devices in the ~~first and~~ third row ~~rows~~.

13. (Original) The DSP architecture of claim 12, further comprising a second communication port connected with at least two memory devices in each of the first, second and third rows of the DSP architecture.

14. (Currently Amended) A DSP (Digital Signal Processing) architecture, comprising:

a first communication port to receive first motion picture image data divided into image frames;

a second communication port to receive second motion picture image data divided into image frames; and

a first arrangement unit connected to the first communication port and the second communication port,

wherein the first arrangement unit comprises first through ~~eight~~ eighth memories to store respective ones of the image frames of the first and second motion picture image data and a calculation element to access the respective image frames of the first through ~~eight~~ eighth memories which are arranged in a matrix structure having three columns and three rows, the second and seventh memories are connected to the second communication port through the calculation element, and the fourth and fifth memories are connected to the first communication port through the calculation element.

15. (Currently Amended) The DSP architecture of claim 14, further comprising:

a third communication port; and

a second arrangement unit connected to the third communication port and to the first and second communication ports through the sixth and the ~~eight~~ eighth memories of the arrangement unit, wherein the second arrangement comprises eight memories and a second calculation element which are arranged in a matrix structure having three columns and three rows.

16. (Original) The DSP architecture of claim 15, further comprising:

a third calculation element and two memories which are disposed between the first and

second arrangement units, wherein the two memories are connected to the memories of the first and second arrangement units through the third calculation element.

17. (Previously Presented) The memory mapping method of claim 11, wherein the data comprises image data divided into at least three image frames such that the storing of the data comprises storing the at least three image frames in the first through the eighth memory devices; and

the processing of the data stored in the first through the eighth memory devices comprises performing an image segmentation process in at least one dimension using the calculation element.

18. (Currently Amended) The DSP architecture of claim 14, wherein the calculation element ~~performs image segmentation on~~ is coupled to the first through the eighth memories to obtain at least one of the first and second motion picture image data stored ~~in the first through the eighth memories~~ therein to subsequently perform image segmentation in at least one dimension thereon.

19. (Withdrawn) A digital signal processing architecture, comprising:

a plurality of memories being a first type of device to store image data; and

a plurality of calculation units being a second type of device different from the first type of device and being arranged among the memories and having a plurality of independent connections to adjacent ones of the memories and to access the adjacent memories and process the image data stored therein.

20. (Withdrawn) The digital signal processing architecture of claim 19, wherein the memories each store image data of one of a previous image frame, a current image frame, or a next image frame.

21. (Withdrawn) The digital signal processing architecture of claim 19, wherein the calculation units perform image segmentation on the image data.

22. (Withdrawn) The digital signal processing architecture of claim 19, wherein each calculation unit moves the stored image data among the adjacent memory devices.

23. (Withdrawn) The digital signal processing architecture of claim 19, further comprising:

at least one communication port disposed adjacent to a first memory, a second memory, and a third memory being connected to the first and third memories and disconnected from the second memory, the at least one communication port receiving the image data and providing the image data to the first and third memories such that a first calculation unit connected to the first, second, and third memories provides the image data from at least one of the first and third memories to the second memory.

24. (Withdrawn) A DSP architecture, comprising:

a communication port to receive image data; and

a plurality of image segmentation units arranged in an array to receive the image data from the communication port, each of the image segmentation units including a plurality of memory devices to store portions of the image data and a calculation unit to retrieve and process the stored portions of the image data.

25. (Withdrawn) The DSP architecture of claim 24, wherein a first one of the image segmentation units receives the image data from the communication port and performs a first segmentation operation on the image data and provides the first segmented image data to a second one of the image segmentation units, and the second one of the image segmentation units performs a second segmentation operation on the first segmented image data to output a second segmented image data.

26. (Withdrawn) The DSP architecture of claim 24, wherein the calculation unit of each of the image segmentation units transfers the stored image data from memory devices of a first image segmentation unit to memory devices of a second image segmentation unit.

27. (Withdrawn) A DSP architecture, comprising:

a plurality of memories being a first type of device to store data;

a plurality of calculation units being a second type of device different from the first type of device and being arranged among the memories having a plurality of connections to directly access adjacent ones of the memories and to process the data stored in the adjacent memories; and

a plurality of communication ports to receive the data and to provide the data to the memories, each communication port being directly connected to at least two memories.

28. (New) A digital processing apparatus, comprising:

a communication port to provide a plurality of image frames;

a plurality of memory units to respectively receive the image frames from the communication port and to respectively store the image frames; and

a calculation element electrically connected directly to each of the memory units and removed from direct connection to the communication port, the calculation element having access to one of the image frames in any of the memory units independently of access to any other of the memory units.

29. (New) The digital processing apparatus of claim 28, further comprising:

another plurality of memory units electrically connected directly to the calculation element to respectively receive processed image frames therefrom; and

another calculation element electrically connected directly to each of the other memory units and removed from direct connection to the communication port, the other calculation element having access to one of the processed image frames in any of the other memory units independently of access to any other of the other memory units.

30. (New) The digital processing apparatus of claim 29, further comprising:

another communication port electrically connected directly to at least one of the plurality of memory units and to one of the other plurality of memory units, the other communication port being removed from direct connection with at least one of the plurality of memory units and from at least one of the other plurality of memory units.

31. (New) A digital processing apparatus, comprising:

a first plurality of memory units interconnected one with another electrically in parallel to be addressed by a communication port;

a second plurality of memory units interconnected one with another electrically in parallel to be addressed by the communication port; and

a calculation element electrically connected directly to the first plurality of memory units and to the second plurality of memory units, the calculation element being electrically remove from direct connection with the communication port and having access to any of the first plurality of memory units and to any one of the second plurality of memory units independently of access to any other of the first plurality of memory units and to any other of the second plurality of memory units.

32. (New) The digital processing apparatus of claim 31, further comprising:

a third plurality of memory units removed from direct connection to the communication port and directly connected to the calculation element to be independently accessed thereby.

33. (New) The digital processing apparatus of claim 31, further comprising:

another calculation element electrically connected directly to the second plurality of memory units and having access to any of the second plurality of memory units independently of access to any other of the second plurality of memory units.